REMARKS

Reconsideration of this application, based on this amendment and these accompanying remarks, is respectfully requested.

Claims 1, 2, 9 through 12, and 14 through 16 remain in this case. Claims 1, 2, 9, 12, 15, and 16 are amended. Claims 7 and 17 through 19 are canceled in this paper, and claims 3 through 6, 8, and 13 were previously canceled.

Claims 18 and 19 were objected to because of certain informalities. These claims are canceled, obviating the objection thereto.

Claims 1, 2, 7, 9, 12, and 14 through 19 were rejected under §102(e) as anticipated by the Abdallah et al. reference[1]. The Examiner asserted that the reference taught all of the elements of claim 1, including the byte intermingling circuitry.[2] Specific teachings directed to the other claims were also found in the reference.[3]

Claim 10, dependent on claim 1, was rejected under §103 as unpatentable over the Abdallah et al. reference in view of the Intel reference[4]. Dependent claim 11 was rejected under §103 as unpatentable over the Abdallah et al. reference in view of the Haataja reference[5].

Amendment is presented to claim 1 to overcome the rejection. Amended claim 1 now recites that the byte intermingling circuitry places data from a first selected field of a single source operand in a lower field of a most significant portion of the destination operand, filling the remainder of the most significant portion of the destination operand with zeroes, and places data from a second selected field of the single source operand, the second selected field being

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[1] U.S. Patent No. 6,115,812, issued September 5, 2000 to Abdallah et al., from an application filed April 1, 1998.
[2] Office Action of October 6, 2004, pages 3 and 4, *citing* Abdallah et al., *supra*, at Figure 3D and column 6, lines 25 through 42.
[3] Office Action, *supra*, pages 3 *et seq.*
[4] *IA-64 Application Developer's Architecture Guide*, (Intel, May 1999).
[5] U.S. Patent No. 6,137,836, issued October 24, 2000, to Haataja.

contiguous with and less significant than the first selected field, in a lower field of a least significant portion of the destination operand, filling the remainder of the least significant portion of the destination operand with zeroes. The specification clearly supports this proposed amendment to claim 1, for example by the examples of the UNPKHU4 and UNPKLU4 instructions, in which data from the single source operand is unpacked and expanded into the destination operand as claimed.[6] Accordingly, no new matter is presented by this proposed amendment to claim 1.

Claims 2 and 9 are amended for consistency with the amendment to claim 1, upon which they depend.

The digital system of proposed amended claim 1 provides important advantages, particularly by way of the byte intermingling recited in the claim that enables the definition of a new instruction. As disclosed in the specification,[7] this instruction simplifies the manipulation of packed data in a microprocessor, thus improving the overall performance of the processor.

Applicants respectfully submit that amended claim 1 and its dependent claims are novel and patentably distinct over the prior art of record.

Regarding the Abdallah et al. reference, upon which the present rejection is based, Applicants submit that this reference fails to disclose the byte intermingling circuitry of amended claim 1. More specifically, Applicants submit that the Abdallah et al. reference fails to disclose circuitry that places data from a first field of the source operand into a lower field of a most significant portion of a destination operation, filling the remainder of that most significant portion with zeroes, and that places data from a second contiguous and less significant field of the source operand into a lower field of a least significant portion of the destination operand, filling the remainder of that least significant portion with zeroes. The cited portion of the reference[8] does not disclose this formation of the destination register contents. And to the

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[6] Specification of S.N. 09/702,405, at page 27, Table 9; page 30, line 25 through page 31, line 5; Figures 6K and 6L.

[7] Specification, *supra*, page 24, line 23 through page 25, line 5.

[8] Abdallah et al., *supra*, column 6, lines 25 through 42; Figure 3D.

extent that the reference discloses placing zeroes into a destination register,[9] these disclosed masking operations necessarily involve the use of a second source operand (the masking registers 560a through 560d), and these disclosed operations fail to result in the recited destination register contents (in which lower fields of most significant and least significant portions contain the source data, with zeroes in the remainder of each of those portions). Accordingly, Applicants submit that amended claim 1 and its dependent claims are novel over the Abdallah et al. reference.

Applicants further respectfully submit that amended claim 1 is novel over each of the references of record in this case, including the Intel and Haataja references applied against claims 10 and 11, respectively, in combination with the Abdallah et al. reference. Attention is also directed to the Philips reference of record, relative to its "packbytes" instruction[10], which requires two source operands and which fails to disclose the arrangement of the destination reference as claimed. Nowhere do any of those references disclose the operation that is required of the byte intermingling circuitry of amended claim 1.

Applicants further respectfully submit that there is no suggestion from the prior art to modify these combined teachings in such a manner as to reach the requirements of amended claim 1. As mentioned above, none of the references disclose the recited operation. And further, to the extent that extraction and zero-filling operations are disclosed,[11] the masking operations require a second mask source operand for the performing of a bit-wise logical AND. There is no suggestion to provide a single instruction that controls byte intermingling circuitry to operate upon a single source operand in the claimed manner. Especially considering the advantages in simplifying data manipulation provided by the claimed system, Applicants respectfully submit that amended claim 1 and its dependent claims are also patentably distinct over the prior art.

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[9] *See* Abdallah et al., *supra*, column 10, lines 46 through 58; Figure 5B.
[10] *TM 1000 Preliminary Data Book* (Philips Electronics, 1997), p. A-138.
[11] *See* Abdallah et al., *supra*, column 10, lines 46 through 58; Figure 5B.

As mentioned above, claims 12 and 14 through 19 were rejected under §102 as anticipated by the Abdallah et al. reference, applied substantially as discussed above relative to claim 1.

Claim 12 is similarly amended to overcome the rejection. Amended claim 12 is directed to a method of operating a digital system, and now requires the writing of data from a first selected field of a single source operand into a lower field of a most significant portion of a destination operand, filling the remainder of the most significant portion with zeroes, and the writing of data from a second contiguous and less significant field of the single source operand into lower field of a least significant portion of the destination operand, filling the remainder of that least significant portion with zeroes. Support for this proposed amendment is clearly present in the specification,[12] and therefore no new matter is presented by this amendment.

Similar important advantages are provided by the method of amended claim 12 and its dependent claims as discussed above relative to claim 1, especially relative to the byte intermingling instruction that operates according to the steps recited in claim 12, specifically by simplifying the manipulation of packed data in a microprocessor, and improving the overall performance of the processor as a result.

Claims 14 through 16 are amended for consistency with amended claim 12, upon which they depend. Claims 17 through 19 are canceled.

Applicants submit that amended claim 12 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

Similarly as discussed above relative to amended claim 1, Applicants submit that the Abdallah et al. reference fails to disclose the writing step of amended claim 12, because the reference fails to disclose the writing of data from a first field of the source operand into a lower field of a most significant portion of a destination operation, filling the remainder of that most significant portion with zeroes, and the writing of data from a second contiguous and less

[12] Specification, *supra*, page 27, Table 9; page 30, line 25 through page 31, line 5; Figures 6K and 6L.

significant field of the source operand into a lower field of a least significant portion of the destination operand, filling the remainder of that least significant portion with zeroes. The portion of the reference cited by the Examiner[13] fails to disclose such writing. And while the Abdallah et al. reference discloses masking operations that fill zeroes into portions of a destination register,[14] these masking operations require a second source operand, and thus do not disclose the use of a single source operand as claimed. Furthermore, the Abdallah et al. reference does not disclose the contents of the destination register resulting from the writing step of amended claim 12, in which lower fields of most significant and least significant portions containing the source data, with zeroes in the remainder of those portions. Accordingly, Applicants submit that amended claim 12 and its remaining dependent claims are novel over the Abdallah et al. reference.

Applicants further respectfully submit that amended claim 12 is not only novel, but is patentably distinct over each of the references of record.

First, none of the references disclose the writing step of amended claim 12. As mentioned above, the writing step of proposed amended claim 12 is not met by the Abdallah et al. reference. Further, also as discussed above relative to claim 1, the Intel, Hennessy, Haataja, Philips, and other references of record in this case also lack disclosure in this regard, and indeed wholly fail to disclose any byte intermingling operations. Accordingly, the combined teachings of the references fall short of the requirements of proposed amended claim 12.

Nor is there suggestion from the prior art to modify these prior art teachings in such a manner as to reach the requirements of amended claim 12. This lack of suggestion is especially evident from the use, in the masked extraction and zero-filling operations that are disclosed,[15] of a second source operand as the mask for the disclosed bit-wise logical AND. There is no suggestion to provide a single instruction that includes the writing step of claim 12. The important advantages provided by the method of amended claim 12, specifically in simplifying

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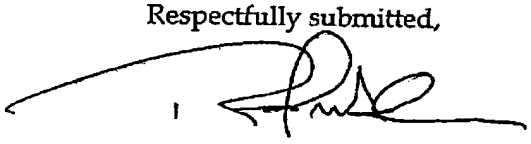
[13] Abdallah et al., *supra*, column 6, lines 25 through 42; Figure 3D.
[14] *See* Abdallah et al., *supra*, column 10, lines 46 through 58; Figure 5B.
[15] *See* Abdallah et al., *supra*, column 10, lines 46 through 58; Figure 5B.

and improving the performance of data manipulation, Applicants respectfully submit that amended claim 12 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

Applicants therefore respectfully submit that amended claim 12 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

Based on the above amendment and these accompanying remarks, Applicants respectfully submit that the claims in this case are now in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,



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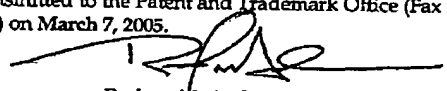

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